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09/992,387	11/16/2001	Anthony L. Coyle	50000.2162	7595
7	7590 02/26/2003			•
GARY C. HONEYCUTT			EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P.O. BOX 655474, MS 3999 DALLAS, TX 75265			LEWIS, MONICA	
DALLAS, IA	73203		ART UNIT	PAPER NUMBER
			2822	· · · · · · · · · · · · · · · · · · ·

DATE MAILED: 02/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

	,	Application No.	Applicant(s)	_
••	Office Action 0	09/992,387	COYLE ET AL.	/
	Office Action Summary	Examiner	Art Unit	<u> </u>
		Monica Lewis	2822	
Period fo	The MAILING DATE of this communication apport	ears on the cover shee	t with th correspondence address	
- Exter after - If the - If NO - Failur - Any re	ORTENED STATUTORY PERIOD FOR REPLY MAILING DATE OF THIS COMMUNICATION. Insions of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. Period for reply specified above is less than thirty (30) days, a reply period for reply is specified above, the maximum statutory period or to reply within the set or extended period for reply will, by statute eply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may within the statutory minimum or will apply and will expire SIX (6) I	y a reply be timely filed thirty (30) days will be considered timely. #IONTHS from the mailing date of this communication	n.
1)[Responsive to communication(s) filed on 09 L	December 2002		
2a)□		is action is non-final.		
3)	Since this application is in condition for allowa		natters prospection as to the movite:	:_
Disposiție	closed in accordance with the practice under on of Claims	Ex parte Quayle, 1935	C.D. 11, 453 O.G. 213.	S
	Claim(s) <u>1-10 and 17-24</u> is/are pending in the	application		
	4a) Of the above claim(s) is/are withdray			
5)	Claim(s) is/are allowed.	on nom consideration.		
	Claim(s) <u>1-10 and 17-24</u> is/are rejected.			
	Claim(s) is/are objected to.			
	Claim(s) are subject to restriction and/or	election requirement		
Application	on Papers	oresten requirement.		
9)[] T	he specification is objected to by the Examiner			
10)□ T	he drawing(s) filed on is/are: a)∐ accep	ted or b) objected to b	the Examiner.	
	Applicant may not request that any objection to the	drawing(s) be held in abo	eyance. See 37 CFR 1.85(a).	
11) <u>⊠</u> T	he proposed drawing correction filed on 13 Nov	<u>/ember 2002</u> is: a)⊠ a	pproved b) \square disapproved by the Exar	mine
12\□ ∓	If approved, corrected drawings are required in repl			
	he oath or declaration is objected to by the Exa	miner.		
	nder 35 U.S.C. §§ 119 and 120			
	Acknowledgment is made of a claim for foreign	priority under 35 U.S.C	. § 119(a)-(d) or (f).	
	All b) Some * c) None of:			
	Certified copies of the priority documents			
	Certified copies of the priority documents			
	B. Copies of the certified copies of the priority application from the International Bure se the attached detailed Office action for a list of the action for a list of	eau (PCT Rule 17 2(a))		
	knowledgment is made of a claim for domestic			n)
a) [\square The translation of the foreign language prov	isional application has	been received	11).
15) L Ac	knowledgment is made of a claim for domestic	priority under 35 U.S.(C. §§ 120 and/or 121.	
ttachment(s	5)			
) 🔲 Notice (of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PTO-948) ation Disclosure Statement(s) (PTO-1449) Paper No(s) <u>6 &</u>	5) Notice o	V Summary (PTO-413) Paper No(s) f Informal Patent Application (PTO-152)	
Patent and Trad	emark Office 04-01) Office Acti		<u>.</u>	

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DETAILED ACTION

1. This office action is in response to the amendment filed December 9, 2002.

Response to Arguments

Applicant's arguments with respect to claims 1-10 and 17-24 have been considered but 2. are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112: 3.
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- Claims 1-10 and 17-24 are rejected under 35 U.S.C. 112, second paragraph, as being 4. indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "exit ports" (See Claim 1, Claim 10 and Claim 17). Claims 2-9 and 18-24 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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6. Claims 1, 2, 4, 5-10, 17, 18 and 20-24 are rejected under 35 U.S.C. 103(a) as obvious over Inaba (Japan Patent No. JP02001217388) in view of Gillette et al. (U.S. Patent No. 5,831,832).

In regards to claim 1, Inaba discloses the following:

- a) an integrated circuit chip (3) having an outline, active and passive surfaces, active components including a plurality of contact pads on said active surface (See Figure 1, Figure 3, Figure 9 and Paragraph 23);
- b) a plurality of electrical coupling members attached to said contact pads, said coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy (See Paragraph 18 and Paragraph 23);
- c) an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface (See Paragraph 16); and
- d) chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface (See Figure 1).

In regards to claim 1, Inaba fails to disclose the following:

a) contact pads spaced apart by less then 100 um.

However, the applicant has not established the critical nature of the dimension of "contact pads spaced apart by less then 100 um." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

b) encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

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However, Gillette et al. ("Gillette") discloses an encapsulant (42) for a ball grid array package (See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include an encapsulant as disclosed in Gillette because it aids in providing protection for the chip (See Figure 2).

Additionally, since Inaba and Gillette are both from the same field of endeavor, the purpose disclosed by Gillette would have been recognized in the pertinent art of Inaba.

In regards to claims 2 and 18, Inaba discloses the following:

a) solder balls attached to said exit ports on said second interposer surface (See Figure 1).

In regards to claims 4 and 20, Inaba discloses the following:

a) interposer is a polyimide film (See Paragraph 16).

In regards to claims 5 and 20, Inaba discloses the following:

- a) interposer has an outline larger than said outline of said chip (See Figure 3). In regards to claims 6 and 22, Inaba discloses the following:
- a) electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold (See Paragraph 15).

In regards to claim 7, Inaba discloses the following:

- a) coupling member is interdiffused with said conductive lines (See Figure 1).

 In regards to claims 8 and 23, Inaba fails to disclose the following:
 - a) encapsulation material is a molding compound.

However, Gillette discloses an encapsulant for a ball grid array package (See Figure 2 and Column 3 Lines 62-63). It would have been obvious to one having ordinary skill in the art at

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the time the invention was made to modify the semiconductor of Inaba to include an encapsulant as disclosed in Gillette because it aids in providing protection for the chip (See Figure 2).

Additionally, since Inaba and Gillette are both from the same field of endeavor, the purpose disclosed by Gillette would have been recognized in the pertinent art of Inaba.

In regards to claims 9 and 23, Inaba fails to disclose the following:

a) molding compound has the same outline as said interposer.

However, Gillette discloses an encapsulant for a ball grid array package (See Figure 2 and Column 3 Lines 62-63). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include an encapsulant as disclosed in Gillette because it aids in providing protection for the chip (See Figure 2).

Additionally, since Inaba and Gillette are both from the same field of endeavor, the purpose disclosed by Gillette would have been recognized in the pertinent art of Inaba.

In regards to claim 10, Inaba discloses the following:

- a) an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface (See Figure 1, Figure 3, Figure 9 and Paragraph 23);
- b) a plurality of electrical coupling members attached to said contact pads, said coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy (See Paragraph 18 and Paragraph 23);
- c) an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface (See Paragraph 16); and
- d) chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface (See Figure 1).

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In regards to claim 10, Inaba fails to disclose the following:

a) encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

However, Gillette discloses an encapsulant for a ball grid array package (See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include an encapsulant as disclosed in Gillette because it aids in providing protection for the chip (See Figure 2).

Additionally, since Inaba and Gillette are both from the same field of endeavor, the purpose disclosed by Gillette would have been recognized in the pertinent art of Inaba.

In regards to claim 17, Inaba discloses the following:

- a) an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface (See Figure 1, Figure 3, Figure 9 and Paragraph 23);
- b) a plurality of electrical coupling members attached to said contact pads (See Paragraph 18 and Paragraph 23);
- c) an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface (See Paragraph 16); and
 - d) chip coupling members interdiffused with said conductive lines (See Figure 1).

 In regards to claim 17, Inaba fails to disclose the following:
- a) encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

However, Gillette discloses an encapsulant for a ball grid array package (See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was

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made to modify the semiconductor of Inaba to include an encapsulant as disclosed in Gillette because it aids in providing protection for the chip (See Figure 2).

Additionally, since Inaba and Gillette are both from the same field of endeavor, the purpose disclosed by Gillette would have been recognized in the pertinent art of Inaba.

7. Claims 3 and 19 are rejected under 35 U.S.C. 103(a) as obvious over Inaba (Japan Patent No. JP02001217388) in view of Gillette et al. (U.S. Patent No. 5,831,832) and Akram (U.S. Patent No. 5,898,224).

In regards to claims 3 and 19, Inaba discloses the following:

a) an adhesive (R) underfilling any spaces between said chip coupling members attached to said conductive lines under said chip (See Figure 1).

In regards to claims 3 and 19, Inaba fails to disclose the following:

a) non-conductive polymer.

However, Akram discloses non-conductive polymer underfilling (See Column 2 Lines 12-18). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include non-conductive polymer underfilling as disclosed in Akram because it aids in reinforcing electrical connections (See Column 2 Lines 12-18).

Additionally, since Inaba and Akram are both from the same field of endeavor, the purpose disclosed by Akram would have been recognized in the pertinent art of Inaba.

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Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML February 14, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800